REMARKS

The Applicant thanks the Examiner for his careful and thoughtful examination of the present application. By way of summary, Claims 1-16 were pending in this application. The claims have not been amended in this Response. Accordingly, Claims 1-16 remain pending for consideration.

DEFECTIVE OATH/DECLARATION

The Office action noted that the declaration submitted with the instant application was defective because it did not identify the mailing address of the inventor, and it did not identify the residence of the inventor. Enclosed herewith, please find a supplemental application data sheet, omitted inadvertently from the originally filed application, containing this missing information, *inter alia*. Since this information has now been submitted in an application data sheet in accordance with § 1.76, Applicant submits that the previously submitted declaration is no longer defective. *See* 37 C.F.R. § 1.63(c).

REJECTION OF CLAIMS 1, 7, 9 AND 15 UNDER 35 U.S.C. § 102(b)

The Office action rejected Claims 1, 7, 9 and 15 under 35 U.S.C. § 102 as being anticipated by U.S. patent application publication no. 2002/0069351, by Chi *et al.* (Chi). Applicant respectfully traverses this rejection because Chi fails to identically teach every element of the claims. See M.P.E.P. § 2131 (stating that in order to anticipate a claim, a prior art reference must identically teach every element of the claim).

For example, Claim 1 recites the steps of "determining if the received data-request is for a non-instruction data if the requested data does not reside in the cache memory . . . and bypassing the cache memory to preserve the contents of the cache memory and provide the fetched non-instruction data to the micro-controller." Chi neither teaches nor discloses such limitations.

The Examiner cites page 3, paragraph [0039] as teaching the step of determining if the received data-request is for a non-instruction data. The Examiner states that Chi "discloses the determining whether instruction is stored in the cache memory and it is inherent that non-instruction data does not reside in the cache memory."

The Examiner's statement that "it is inherent that non-instruction data does not reside in the cache memory" is without support in Chi, or any of the other references cited by the Examiner. Moreover, the Examiner's statement is contradicted by Applicant's statements in the Background of the Invention: "a cache control system is frequently included which minimizes access time for fetching instructions and data from memory;" and "[i]n prior art cache systems, a so-called "Harvard" architecture has been used which attempts to solve the foregoing problem by providing separate cache structures for instructions and data." (Emphasis added.) *Also see, e.g.,* http://www.arm.com/support/faqip/3738.html (describing cache systems that cache both instructions and data). The Applicant submits that it is not inherent or well-known that "non-instruction data does not reside in the cache memory," and requests that the Examiner provide adequate evidence to support this finding. *See* M.P.E.P. § 2144.03 ("If Applicant challenges a factual assertion as not properly officially noticed or not properly based upon common knowledge, the Examiner must support the finding with adequate evidence").

Moreover, in paragraph [0039], Chi only discloses that "the cache memory 301 determines whether the missed instruction, that is, the instruction not stored in the cache memory 301 such as I_3 introduced in prior art, should be fetched from an external memory." Chi never discloses determining if the received data-request is for non-instruction data. Therefore, Chi does not disclose or suggest the step of determining if the received data-request is for non-instruction data.

With respect to the "bypassing" limitation of Claim 1, the Examiner cites paragraphs [0037] and [0039] of Chi, stating that Chi "discloses the cache memory for instruction and it is inherent that non-instruction data would not be stored in this cache memory and preserve the contents of the cache memory." As with respect to the determining limitation, Applicant submits that it is not inherent or well-known that "non-

instruction data would not be stored in this cache memory," and requests that the Examiner provide adequate evidence to support this finding. *See* M.P.E.P. § 2144.03 ("If Applicant challenges a factual assertion as not properly officially noticed or not properly based upon common knowledge, the Examiner must support the finding with adequate evidence"). Applicant finds no disclosure or suggestion in Chi that suggests the step of bypassing the cache memory to provide the fetched non-instruction data to the micro-controller.

For at least these reasons, the rejection of Claim 1 as anticipated by Chi is improper.

Claim 9 recites a micro-controller cache system adapted to "determine if the received data-request is for a non-instruction data if the requested data does not reside in the cache memory . . . and bypass the cache memory to preserve the contents of the cache memory and provide the fetched non-instruction data to the micro-controller." Chi neither teaches nor discloses such a system.

For reasons similar to those discussed above with respect to Claim 1, Applicant submits that it is not inherent or well-known that "non-instruction data would not be stored in this cache memory," and requests that the Examiner provide adequate evidence to support his assertions that Chi discloses the above limitations. *See* M.P.E.P. § 2144.03 ("If Applicant challenges a factual assertion as not properly officially noticed or not properly based upon common knowledge, the Examiner must support the finding with adequate evidence"). Applicant submits that Chi does not disclose a cache system adapted to determine if the received data-request is for a non-instruction data and bypass the cache memory to provide the fetched non-instruction data to the micro-controller.

In paragraph [0039], Chi discloses that "the cache memory 301 determines whether the missed instruction, that is, the instruction not stored in the cache memory 301 such as I_3 introduced in prior art, should be fetched from an external memory." Yet, Chi never discloses determining if the received data-request is for non-instruction data. Therefore, Chi does not disclose or suggest a cache system adapted to determine if the received data-request is for non-instruction data.

For at least these reasons, the rejection of Claim 9 as anticipated by Chi is improper.

Claims 7 and 15 which depend from Claims 1 and 9 respectively, are believed to be patentable for the same reasons articulated above with respect to Claims 1 and 9, and because of the additional features recited therein.

REJECTION OF CLAIMS 1-3, 7, 9-11 AND 15 UNDER 35 U.S.C. § 103(a)

The Office action rejected Claims 1-3, 7, 9-11 and 15 under 35 U.S.C. § 103 as being unpatentable over U.S. patent no. 6,647,463, issued to Yamashiroya (Yamashiroya), and U.S. patent no. 6,922,754, issued to Liu *et al.* (Liu).

REFERENCES FAIL TO TEACH ALL OF THE CLAIMED ELEMENTS

The Applicant respectfully traverses this rejection because Yamashiroya, alone or in combination with Liu, fails to teach or suggest all of the elements of the claims. *See* M.P.E.P. § 2143 (stating that in order to establish a *prima facie* case of obviousness for a claim, the prior art references must teach or suggest all the claim limitations).

For example, Claim 1 recites the steps of "determining if the received data-request is for a non-instruction data if the requested data does not reside in the cache memory . . . and bypassing the cache memory to preserve the contents of the cache memory and provide the fetched non-instruction data to the micro-controller." Yamashiroya, by itself or in combination with Liu, fails to teach or suggest these limitations.

The Examiner cites Column 6, lines 4-12 of Yamashiroya as teaching the step of determining if the received data-request is for a non-instruction data. However, this portion of Yamashiroya is not concerned with non-instruction data, and does not disclose the step of determining if the received data-request is for non-instruction data. Instead, Yamashiroya, in this passage, simply teaches the step of determining whether or not a cache miss has occurred, without regard for whether the received data-request is for non-instruction data. No other portion of Yamashiroya teaches or suggests this limitation of "determining if the received data-request is for a non-instruction data if the

requested data does not reside in the cache memory." Liu also does not teach or suggest the step of determining if the received data-request is for a non-instruction data, and so the combination of these references fails to teach or suggest this limitation.

With respect to the "bypassing" limitation of Claim 1, the Examiner cites Column 1, lines 47-56 and Column 10, lines 23-35 of Liu, stating that Liu "discloses bypassing the cache memory based on many factors including type of data request and it is obvious non-instruction data may be the type of data for bypassing based on locality of reference." Yet, in the cited passages, Liu's only examples of bypassing the cache memory are for no write-back caching, for caching only certain volumes, for not caching data intended for certain LUNs, for not caching when a cache stress exceeds a threshold, and for not caching large reads and writes. Applicant submits that, without relying on Applicant's teaching in the instant application, it would not have been obvious that "non-instruction data may be the type of data for bypassing," and requests that the Examiner provide adequate evidence to support this finding. *See* M.P.E.P. § 2144.03 ("If Applicant challenges a factual assertion as not properly officially noticed or not properly based upon common knowledge, the Examiner must support the finding with adequate evidence"). Applicant finds no disclosure or suggestion in Liu that teaches or suggests the step of bypassing the cache memory to provide the fetched non-instruction data to the micro-controller. Moreover, as admitted by the Examiner, Yamashiroya also fails to teach this step, and so the combination of these references fails to teach or suggest this limitation.

For at least these reasons, the rejection of Claim 1 as obvious in view of Yamashiroya and Liu is improper.

Claim 9 recites a micro-controller cache system adapted to "determine if the received data-request is for a non-instruction data if the requested data does not reside in the cache memory . . . and bypass the cache memory to preserve the contents of the cache memory and provide the fetched non-instruction data to the micro-controller." Yamashiroya, alone or in combination with Liu, fails to teach or suggest such a system.

For reasons similar to those discussed above with respect to Claim 1, Applicant submits that neither Yamashiroya nor Liu, nor the combination of these references,

teaches or suggests a cache system adapted to determine if the received data-request is for a non-instruction data if the requested data does not reside in the cache memory and bypass the cache memory to provide the fetched non-instruction data to the micro-controller.

Claims 2, 3, 7, 10, 11 and 15 which depend from one of Claims 1 and 9, are believed to be patentable for the same reasons articulated above with respect to Claims 1 and 9, and because of the additional features recited therein.

NO SUGGESTION TO COMBINE YAMASHIROYA AND LIU

The Examiner has also not established that one of ordinary skill in the art would have combined the teachings of Yamashiroya and Liu. Furthermore, the Examiner has not established that one of ordinary knowledge would have combined these references to meet the limitations of the claimed inventions.

Section 2143 of the M.P.E.P. states that to establish prima facie obviousness three requirements must be met:

> "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure."

In the present case, Yamashiroya discloses "a cache having a high speed and a small capacity . . . mounted between a processor core and a main memory so that an access to data stored in the main memory can be made faster." Col. 1, ll. 14-17. Meanwhile, Liu discloses a cache system in a "data-aware data flow manager (DADFM) . . . inserted between storage and a process or device requesting access to the storage." Col. 1, ll. 42-44. In particular, this DADFM disclosed by Liu is not mounted between a processor core and memory, but is rather "incorporated on a network

appliance that sits between a mass storage device and a device that requests access to the data on the storage device [or] in an output driver layer of an operating system or an application executing on the device." Col. 2, ll. 28-36. Figure 3 of Liu clearly shows the DADFM 120 external to and between a server 105 and storage 125. There is no suggestion or motivation to combine the teachings of Liu's external cache system with the teachings of Yamashiroya relating to a cache between a processor core and a main memory.

With respect to the motivation to combine, the Office action asserts that Liu "states that through intelligent management and caching of data flow, invention is able to avoid some of the latencies associated with cache (column 1, lines 49-52)." However, Applicant submits that the Office action mis-quotes Liu, who states in this section that "[t]hrough intelligent management and caching of data flow, the data-aware data flow manager is able to avoid some of the latencies associated with caches that front storage devices." In other words, Liu teaches the advantages of ameliorating the response times of mass storage devices, a problem irrelevant to the disclosure of Yamashiroya.

It appears that the Examiner has impermissibly used hindsight derived from the teachings in the present application, and not the teachings of the prior art, to reject the above claims. In re Dembiczak, 175 F.3d 994, 999 (Fed. Cir. 1999) (holding the Board impermissibly used hindsight in determining obviousness); *See, also*, M.P.E.P. § 2145, part X.A. In Dembiczak, the Federal Circuit reiterated that a determination of obviousness cannot simply rely on the inventor's disclosure as a "blueprint" without evidence of a suggestion, teaching or motivation in the prior art. Dembiczak, 175 F.3d 994, 999. Also, according to M.P.E.P. § 706.02(j), "[t]he teaching and suggestion to make the claimed combination and the reasonable expectation for success must both be found in the prior art and not based on the Applicant's disclosure." (emphasis added).

REJECTION OF CLAIMS 4-6, 8, 12-14 AND 16 UNDER 35 U.S.C. § 103(a)

The Office action rejected Claims 4-6, 8, 12-14 and 16 under 35 U.S.C. § 103 as being unpatentable over Yamashiroya, Liu and further in view of U.S. patent application publication no. 2002/0065994, by Henson *et al.* (Henson).

REFERENCES FAIL TO TEACH ALL OF THE CLAIMED ELEMENTS

The Applicant respectfully traverses this rejection because Yamashiroya, alone or in combination with Liu and Henson, fails to teach or suggest all of the elements of independent Claims 1 and 9, as discussed above. *See* M.P.E.P. § 2143 (stating that in order to establish a *prima facie* case of obviousness for a claim, the prior art references must teach or suggest all the claim limitations). Henson does not teach any of the limitations discussed above that were not taught or suggested by Yamashiroya and Liu.

Claims 4-6, 8, 12-14 and 16, which depend from Claims 1 and 9, are therefore believed to be patentable for the same reasons articulated above with respect to Claims 1 and 9, and because of the additional features recited therein.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the pending claims are now in condition for allowance and requests reconsideration of the rejections. If it is believed that a telephone conversation would expedite the prosecution of the present application, or clarify matters with regard to its allowance, the Examiner is invited to contact the undersigned attorney at the number listed below.

The Commissioner is hereby authorized to charge payment of any required fees associated with this Communication or credit any overpayment to Deposit Account No. 23-1209.

Respectfully submitted,

Date: January 16, 2005

By: _____
Jason T. Evans, Esq.
Reg. No. 57,862

WESTERN DIGITAL TECHNOLOGIES, INC.
20511 Lake Forest Drive
Lake Forest, CA 92630
Tel.: (949) 672-7000
Fax: (949) 672-6604